100G CWDM4 TOSA 光发射组件

产品描述

100Gbps CWDM4 TOSA光器件可用于研制和生产制造100G QSFP28 CWDM4光收发模块，是模块中用于发射的光组件。TOSA光组件采用封闭盒式封装，内部集成了4CH激光器芯片，LDD激光器驱动，MUX复用器芯片和I2C电路。外部采用封闭盒式更有利于电子射频信号，SMT工艺焊盘接口进行外部PCB连接。

注：M-LD

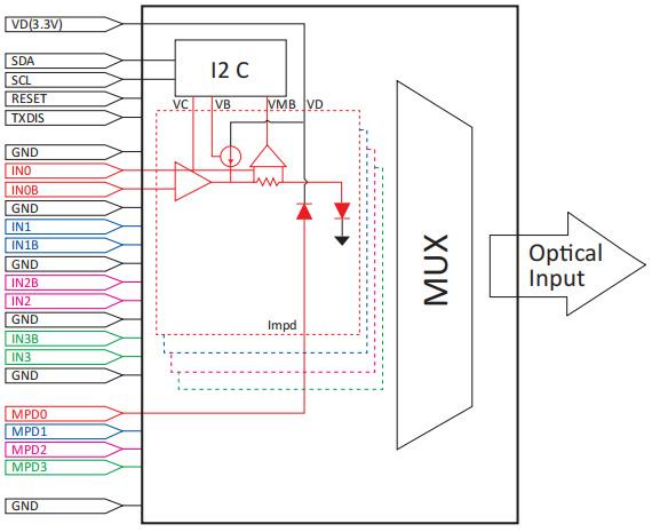
产品特点

- 单波长速率可达25.78125Gb/s±1000ppm(NRZ)
- 1270nm、1290nm、1310nm、1330nm 4波长DML激光器芯片
- 集成LDD激光器驱动器
- 推荐CDR型号为M37049G-16
- 高达400kHz的双线通信
- 集成CWDM4 MUX芯片
- LC尾纤连接器
- 更有利于射频电信号的SMT工艺焊接
- 兼容40G CWDM4光模块

产品应用

- CWDM4 MSA
- 研制100G QSFP28 CWDM4光收发模块
- 研制40G QSFP CWDM4光收发模块
- QSFP28/CFP2/CFP4光收发模块

Modular Block Diagram



Absolute Maximum Ratings Tc = 25°C, (unless otherwise specified)

Parameter	Symbol	Condition	Min.	Max.
Supply Voltage	VD		-0.3 V	3.6 V
Data Input Amplitude	IN0~3	AC coupled		2.5 Vppd
Monitor Photodiode Forward Current	Impd_f			10 mA
Monitor Photodiode Reverse Voltage			20 V	
Storage Temperature	Tstg		-40 degC	85 degC
Electrical Discharge Voltage(HBM)	VESD,HBM			TBD

Optical and Electrical Characteristics Tc = 0°C to 80°C, (unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.
Bit Rate		NRZ, each lane		25.781 Gb/s	
Operational Case Temperature	Tc		0℃	25℃	80℃
Laser					
Peak Wavelength for L0	L_0[1]	for L0	1264.5 nm	1271 nm	1277.5 nm
	L_1[1]	for L1	1284.5 nm	1291 nm	1297.5 nm
	L_2[1]	for L2	1304.5 nm	1311 nm	1317.5 nm
	L_3[1]	for L3	1324.5 nm	1331 nm	1337.5 nm
Average Output Power	P_f	each lane[1]	-6.5 dBm	0.0 dBm	2.5 dBm
Total Average Launch Power	P_T				8.5 dBm
Optical Modulation Amplitude	P_{OMAI}	each lane[1]	-4[2] dBm	-0.65 dBm	2.5 dBm
Extinction Ratio[1]	E_R		3.5 dB		
Optical Return Loss Tolerance	O_{RL}				20 dB
Transmitter Reflectance	T_R				-12[3] dB
Side-mode Suppression Ratio	SSR		30 dB		
Transmitter and Dispersion Penalty	T_{DP}	each lane, SMF = 2 km			3.0[4] dB
Transmitter eye mask definition (X1, X2, X3, Y1, Y2, Y3)[1, 4, 5]		4th Bessel		Refer to Figure1 (0.31, 0.4, 0.45, 0.34, 0.38, 0.4)	
Mask Margin	MM	5E-5			
Monitor PD					
Monitor PD Current	Impd	Pf = 0 dBm	TBD		TBD
Reverse Voltage	Vrp	Pf = 0 dBm	1.5 V		
I2C / Driver					
Supply Voltage	VD		2.97 V	3.3 V	3.47 V
Supply Current	ID			TBD	TBD
DML Bias Current	IBIAS				70 mA
DML Bias Control Voltage	VB0~3				2.5 V
Modulation Control Voltage	VC0~3				2.5 V
Cross Point Control Voltage	VX0~3				1.0 V
Data Input Amplitude	IN	AC coupled	0.7 Vppd		1.5 Vppd
Input Logic Voltage High[6]	VIH	SDA, SCL, RESET, TXDIS	1.3 V	0 V	3.47 V
Input Logic Voltage Low[6]	VIL	SDA, SCL, RESET, TXDIS	0 V	0 V	0.4 V
Output Logic Voltage High[6]	VOH	SDA, I_{OH} = I_{OL}= 4 mA	1.5 V	1.7 V	1.92 V
Output Logic Voltage Low[6]	VOL	SDA, I_{OH} = I_{OL}= 4 mA		0 V	0.3 V
Total Power Dissipation	Ptotal			TBD	TBD

1: 25.8 Gbps, PRBS = 231-1.
2: Even if the TDP < 1.0dB, the OMA (min) must exceed this value.
3: Transmitter reflectance is defined looking into the transmitter.
4: TDP does not include a penalty for multi-path interference (MPI).
5: See mark in Figure 1.
6: See recommended circuit in Figure 2.

Figure 1. SRS Eye Mask

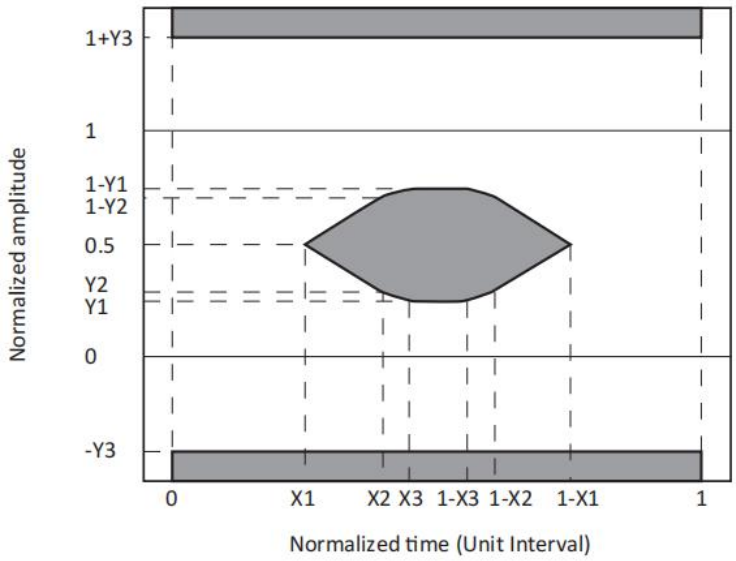
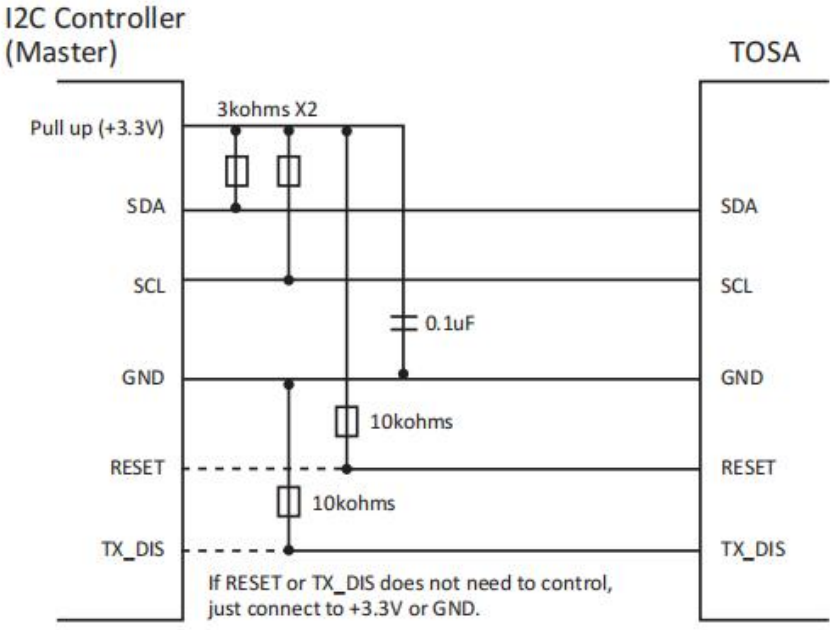
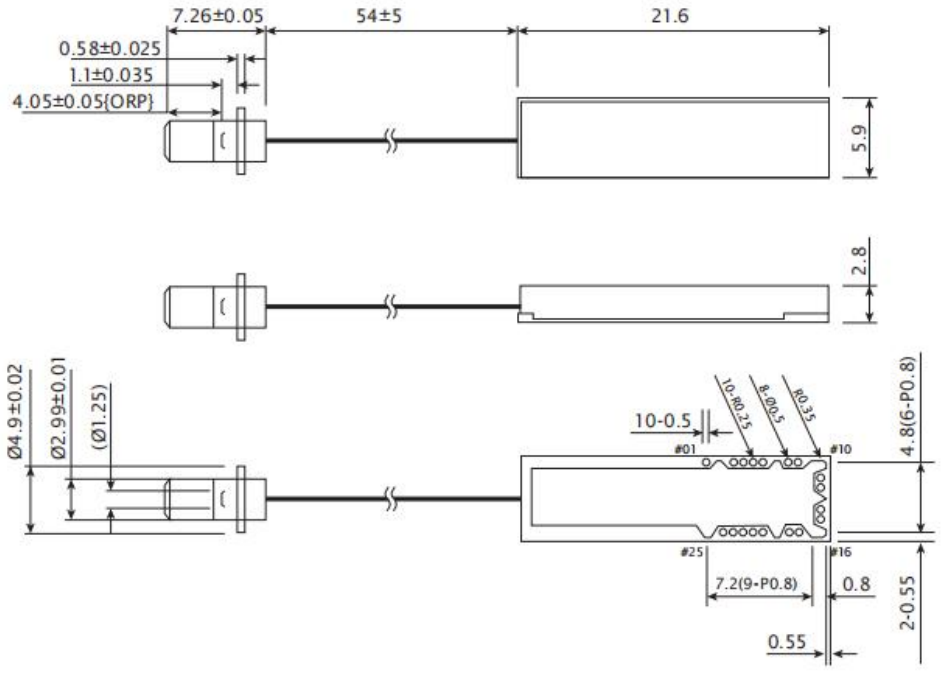


Figure 2. Recommended Circuit



Dimensions



Unit: mm

Pin Configuration

Pin#	Symbol	Description
1	N/C	No Connection
2,7,10,13,16,19,25	GND	Ground
3	MPD0	Monitor PD anode for L0
4	MPD1	Monitor PD anode for L1
5	MPD2	Monitor PD anode for L2
6	MPD3	Monitor PD anode for L3
8	IN3B	Negative data input for L3
9	IN3	Positive data input for L3
11	IN2B	Negative data input for L2
12	IN2	Positive data input for L2

Pin#	Symbol	Description
14	IN1	Positive data input for L1
15	IN1B	Negative data input for L1
17	IN0	Positive data input for L0
18	IN0B	Negative data input for L0
20	SDA	Two-wire serial interface data
21	SCL	Two-wire serial interface clock
22	TXDIS	Global power down for disable, active high
23	VD	+3.3 Voltage Power Supply
24	RESET	Reset signal, active high

注：产品技术规格如有变更，恕不另行通知，如有疑议，请与我司联系。

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