

100G CWDM4 ROSA 光接收组件



产品描述

100Gbps CWDM4 ROSA光组件可用于研制和生产制造100G QSFP28 CWDM4光收发模块，是光模块中用于光信号接收的光组件。ROSA光组件采用封闭盒式封装，内部集成了 TIA+LA+CDR电芯片，集成了4CH PIN PD光探测芯片，同时集成了4CH CWDM4 De-MUX 光信号解复用器芯片。采用SMT工艺焊盘接口与外部PCB连接。

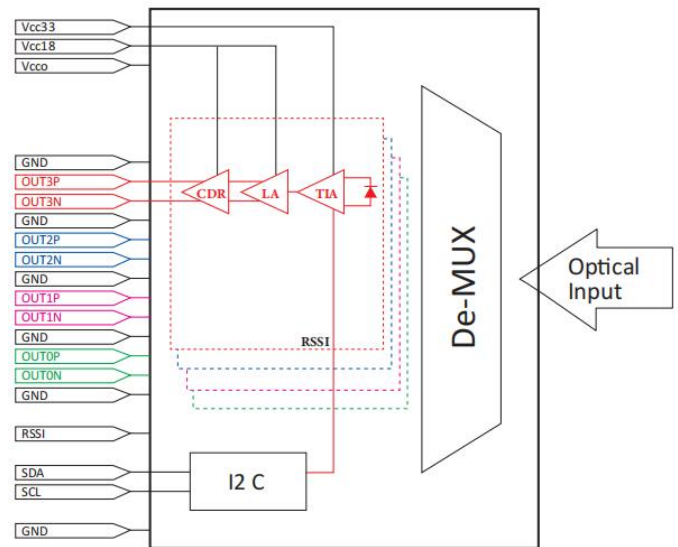
产品特点

- 单波长速率可达25.78125Gb/s±1000ppm(NRZ)
- 集成4通道PIN-PD光探测芯片
- 集成电芯片 TIA+LA+CDR
- 可编程输出 Swing, Squelch, De-Emphasis
- 高达400kHz的双线通信
- 集成CWDM4 De-MUX芯片
- LC尾纤连接器
- 更有利于射频电信号盒式封装，SMT工艺焊接连接PCB
- 兼容40G CWDM4光模块

产品应用

- CWDM4 MSA
- 研制100G QSFP28 CWDM4光收发模块
- 研制40G QSFP CWDM4光收发模块
- QSFP28/CFP2/CFP4光收发模块

Modular Block Diagram



Absolute Maximum Ratings Tc = 25°C, (unless otherwise specified)

Parameter	Symbol	Condition	Min.	Max.
Maximum Optical Input Power	PIN	Each lane, CW	4 dBm	
Core Power Supply Voltage (1.8V)	Vcc18, Vcco		-0.5 V	2 V
TIA Power Supply Voltage (3.3V)	Vcc33		-0.5 V	4 V
DC Input Voltage (CMOS)	VIN CMOS	SCL	GND-0.5 V	3.8 V
Maximum Current from RSSI	IRSSI		4 mA	
Maximum Current from OUTP/N	Iout		20 mA	
Storage Temperature	Tstg		-40 degC	85 degC
Electrical Discharge Voltage(HBM)	VESD, HBM			TBD

Optical and Electrical Characteristics Tc = 0°C to 80°C, (unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.
Bit Rate		NRZ, each lane		25.781 Gb/s	
Operational Case Temperature	Tc		0°C	25°C	80°C
PD					
Peak Wavelength for L0	L ₀ ¹	for L0	1264.5 nm	1271 nm	1277.5 nm
	L ₁ ¹	for L1	1284.5 nm	1291 nm	1297.5 nm
	L ₂ ¹	for L2	1304.5 nm	1311 nm	1317.5 nm
	L ₃ ¹	for L3	1324.5 nm	1331 nm	1337.5 nm
PD Responsivity	R	CW	TBD	TBD	TBD
Damage threshold, each lane ²	P _d	CW	3.5 dBm		
Maximum Overload, each lane ¹	P _{max}	OMA	2.5 dBm		
Minimum Sensitivity, each lane ^{1, 3}	P _{min}	OMA		-10 dBm	
SRS eye mask definition (X1, X2, X3, Y1, Y2, Y3) ^{1, 4, 5}		4 th Bessel		Refer to Figure1 (0.39, 0.5, 0.5, 0.39, 0.39, 0.4)	
Optical Return Loss	ORL	λ = 1300 nm			26 dB
TIA/LA/CDR					
Core Power Supply Voltage (1.8 V)	Vcc18, Vcco		1.71 V		3.47 V
TIA Power Supply Voltage (3.3 V)	Vcc33		2.97 V		3.47 V
Differential Output Impedance Termination	R _{TERM}				
Differential Output Amplitude ⁸	R _{XX}	AC	300mVppd		930 mVppd
Rx x Rise/Fall Time ¹²	T _{RISE} /T _{FALL}	20~80%			20 psec
Output Differential Return Loss ⁶	S22				TBD
RSSI Range	RSSI _{Range}		4 μA		504 μA
Program Output De-emphasis ^{8, 12}	DE		0 dB		7.5 dB
Total Output Jitter ¹⁰	t _{JIT}				TBD
Loss Of Signal ^{7, 8}	LOS				TBD
LOS Hysteresis ^{7, 8}	LOS _{HYST}		1.5 dB		2.5 dB
LOS Assert Time ⁹	T _{ast}				100 μsec
LOS De-assert Time ⁹	T _{deast}				100 μsec
CDR Lock Time	T _{LOCK}			0.7 msec	2 msec
LOL Timing from occurrence to triggering ¹¹	T _{LOCK}				0.5 msec

Optical and Electrical Characteristics $T_c = 0^{\circ}\text{C}$ to 80°C , (unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.
I2C					
CMOS Output Logic High	V_{OH_CMOS}	$I_{OH} = 4\text{ mA}$	1.5 V	1.7 V	1.92 V
CMOS Output Logic Low	V_{OL_CMOS}	$I_{OH} = 4\text{ mA}$		0 V	0.3 V
Open Drain Output Logic High	V_{OH_OD}	$I_{OH} = 4\text{ mA}$	$0.8 \times V_{CC_EXT}$		V_{CC_EXT}
Open Drain Output Logic Low	V_{OL_OD}	$I_{OH} = 4\text{ mA}$		0 V	0.3 V
Input Logic High	V_{IH}		$0.75 \times V_{CC18}$		3.465 V
Input Logic Low	V_{IL}		0 V		$0.2 \times V_{CC18}$
Total Power Dissipation	P_{total}			0.71 W	TBD

1: 25.8Gbps, PRBS=231-1.

2: The receiver shall be able to tolerate, without damage, continuous exposure to an optical signal having this average power level.

3: BER=5E-5 and normative specification.

4: BER=5E-5, Vertical eye closure penalty = 1.9 dB, J2 Jitter = 0.33 UI and J4 Jitter = 0.48 UI.

5: See mark in Figure1.

6: Measured using MACOM EVM and an output latched high or low.

7: The LOS assert/de-assert levels are independent of CDR enable or CDR bypass modes.

8: Typical programmable range.

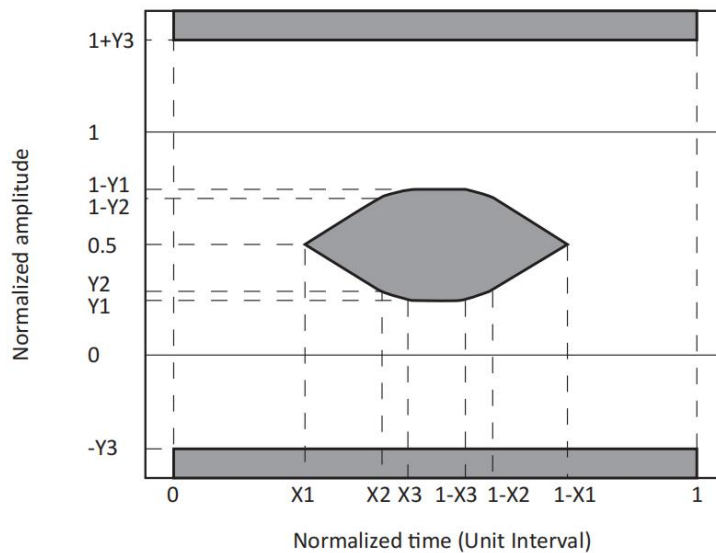
9: Minimum of 6 dB change in optical signal.

10: CDR enabled.

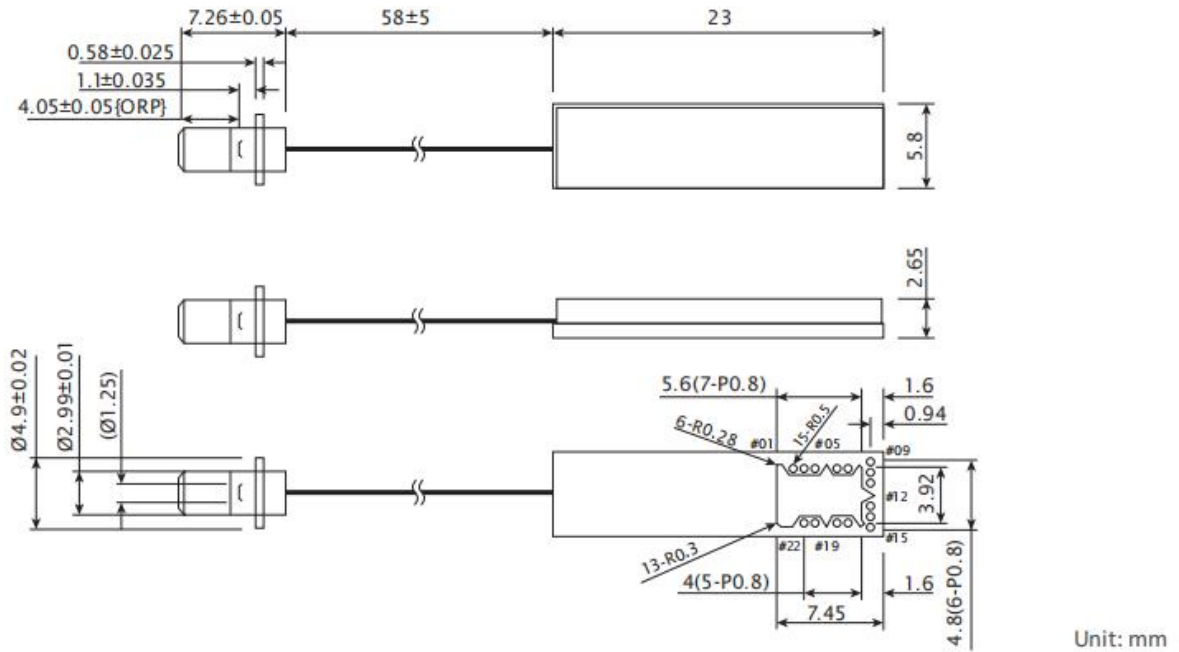
11: The time it takes to assert the LOL from valid input data to invalid input data. The valid input data is data within range covered by the data rates.

12: Measured with 100 Ω differential load.

Figure 1. SRS Eye Mask



Dimensions



Pin Configuration

Pin#	Symbol	Description
1,5,8,9,12,15,16,19,22	GND	Ground
2	Vcc33	+3.3 V power supply
3	NC	No Connect
4	Vcco	+1.8 V power supply
6	OUT3P	positive data output for L0
7	OUT3N	negative data output for L0
10	OUT2P	positive data output for L1

Pin#	Symbol	Description
11	OUT2N	negative data output for L1
13	OUT1P	positive data output for L2
14	OUT1N	negative data output for L2
17	OUT0P	positive data output for L3
18	OUT0N	negative data output for L3
20	SCL	two-wire serial interface clock
21	SDA	two-wire serial interface data

注：产品技术规格如有变更，恕不另行通知，如有疑问，请与我司联系。

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